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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,886	09/30/2003	Hyunjun Kim	P16828	9223

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Buckley, Maschoff, Talwalkar & Allison LLC
Five Elm Street
New Canaan, CT 06840

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/674,886	KIM ET AL.
	Examiner	Art Unit
	Jeremy C. Norris	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Based on the Pre-Appeal Brief Review, the previous Final Rejection has been withdrawn and the submission dated 25 November 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3, 5, 7-10, 12-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,172,305 (Tanahashi)

Tanahashi discloses, referring to figures 3a-c, an apparatus, comprising: a first voltage plane (12) having a first conducting portion (P2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (G1) to be at a second voltage; and a plurality of floating microstrip line traces (G4 one shown, a plurality referred to, see col. 16, lines 55-60) on the signal layer. While Tanahashi does specifically show one microstrip line electrically connected to the second conducting portion at a first end (via T2) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second conducting portion at the second end, Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion [claims 1, 14, 18]. However, it would have been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

Additionally, the modified invention of Tanahashi teaches wherein the first voltage plane is a power plane (P2) and the second voltage plane is a ground plane (G1) [claim 2], wherein the microstrip line and the second voltage plane are electrically connected via a plated through hole (T2) [claim 5], wherein the microstrip line provides impedance damping (see col. 2, lines 60-65) [claim 7], wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane (see col. 2, line 60 – col. 3, line 5) [claims 8, 19], wherein the first voltage plane, the signal layer, and the second voltage plane are separated by a dielectric material (14, 13) [claim 9], wherein the apparatus is a printed circuit board and the microstrip lines are positioned substantially around the perimeter of the board [claim 10], further comprising: a second signal layer (S1) [claim 12] and positioning the microstrip line in the signal layer to reduces cross-talk (see col. 6, lines 20-35) [claim 15]

.

Moreover, although the modified invention of Tanahashi does not specifically state a plurality of second microstrip lines each microstrip line is electrically connected to the second voltage plane at a first end (see col. 17, lines 45-60) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second voltage plane at the second end [claims 13, 16], such a modification would only involve creating a signal layer substantially identical to the signal layer previously described. Since Tanahashi clearly teaches adding additional layers similar to the explicitly described layers to the invention (col. 16, lines 50-60), it would have been obvious to one having ordinary skill in the art at the time of invention

to add such a signal layer. The motivation for doing so would have been to allow for more signal routing. Additionally, it would have been obvious to one having ordinary skill in the art at the time of invention to connect the microstrip lines to the same voltage plane. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

Similarly, regarding claims 1 & 3, Tanahashi discloses, referring to figures 3a-c, an apparatus, comprising: a first voltage plane (12) having a first conducting portion (G2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (P1) to be at a second voltage; and a plurality of floating microstrip line traces (P4 one shown, a plurality referred to, see col. 16, lines 55-60) on the signal layer. While Tanahashi does specifically show one microstrip line electrically connected to the second conducting portion at a first end (via T5) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second conducting portion at the second end, Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion [claims 1, 14]. However, it would have been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow. Also, Tanahashi

teaches wherein the first voltage plane is a ground plane (G2) and the second voltage plane is a power plane (P1) [claim 3].

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanahashi as applied to claim 1 above, and further in view of US 6,188,296 (Nibe).

Tanahashi teaches the claimed invention as described above except Tanahashi does not specifically state that each microstrip line is substantially 15μm thick. However, it is well known in the art to form microstrip lines with this thickness as evidenced by Nibe (see col. 7, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form each microstrip line in the invention of Tanahashi to be 15μm thick as is known in the art and evidenced by Nibe. The motivation for doing so would have been to tailor the characteristic impedance to a desired value. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanahashi as applied to claim 10 above, and further in view of US 6,288,900 (Johnson).

Tanahashi discloses the claimed invention as described above except Tanahashi does not specifically state the printed circuit board is associated with at least one of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model (col. 4, lines 5-20) [claim 11]. Instead Tanahashi generically states that the board is to be

associated with "a semiconductor integrated circuit device". Flip chip ball grid arrays (FC/BGA) are well known semiconductor integrated circuit devices as evidenced by Johnson (see col. 1, lines 1-5). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to replace the generic "semiconductor integrated circuit device" of the invention of Tanahashi with a FC/BGA as is well known in the art and evidenced by Johnson. The motivation for doing so would have been to use a package with a small footprint thus not needlessly squandering board space.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,243,261 (hereafter Janik) in view of Tanahashi.

Janik discloses a PCB coupled to a DRAM [claim 20] and a processor [claim 21]. Janik does not disclose the particulars of the PCB. Tanahashi teaches, referring to figures 3A-C, a first voltage plane (11) having a first conducting portion (G2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (G1) to be at a second voltage and a plurality of floating microstrip line traces (G4) on the signal layer. Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the PCB taught by Tanahashi in the invention of Janik. The motivation for doing so would have been to use a circuit board with enhanced protection against cross talk, resulting in a more reliable device. Janik in view of Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion. However, it would have

been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 7-16, and 18-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800